WHAT IS CLAIMED IS:

1. A method of forming a metal interconnect in an integrated circuit, the method comprising the steps of:

forming a copper layer over dielectric structures on the integrated circuit, where the dielectric structures have an upper level,

planarizing the copper layer to be no higher than the upper level of the dielectric structures, without reducing the upper level of the dielectric structures, and

forming an electrically conductive capping layer over all of the copper layer, without the capping layer forming over any of the dielectric structures.

2. The method of claim 1, wherein the step of forming the copper layer comprises forming the copper layer using electrochemical deposition.

3. The method of claim 1, wherein the step of planarizing the copper layer comprises electrochemical polishing of the copper layer.

4. The method of claim 1, wherein the step of forming the electrically conductive capping layer comprises electroless deposition of the electrically conductive capping layer.

5. The method of claim 1, wherein the dielectric structures comprise low k materials.

6. The method of claim 1, wherein the electrically conductive capping layer comprises cobalt.

7. The method of claim 1, wherein the electrically conductive capping layer comprises nickel.

8. The method of claim 1, further comprising the step of forming an inter metallic dielectric layer over the electrically conductive capping layer and the dielectric structures.

9. A metal interconnect formed according to the method of claim 1.

10. An integrated circuit having a metal interconnect formed according to the method of claim 1.

11. A method of forming a metal interconnect in an integrated circuit, the method comprising the steps of:

forming a copper layer over dielectric structures on the integrated circuit, where the dielectric structures have an upper level, the copper layer formed using electrochemical deposition,

planarizing the copper layer to be no higher than the upper level of the dielectric structures, without reducing the upper level of the dielectric structures, the copper layer planarized using electrochemical polishing, and

forming an electrically conductive capping layer over all of the copper layer, without the capping layer forming over any of the dielectric structures, the electrically conductive capping layer formed using electroless deposition.

12. The method of claim 11, wherein the dielectric structures comprise low k materials.

13. The method of claim 11, wherein the electrically conductive capping layer comprises cobalt.

14. The method of claim 11, wherein the electrically conductive capping layer comprises nickel.

15. The method of claim 11, further comprising the step of forming an inter metallic dielectric layer over the electrically conductive capping layer and the dielectric structures.

16. A metal interconnect formed according to the method of claim 11.

17. An integrated circuit having a metal interconnect formed according to the method of claim 11.

18. In an integrated circuit, the improvement comprising a metal interconnect including:

a copper layer formed between dielectric structures, where the dielectric structures have an upper level, where the upper level of the dielectric structures is substantially uniform across all of the dielectric structures,

the copper layer planarized to be no higher than the upper level of the dielectric structures, the copper layer having no dishing between the dielectric structures, and

an electrically conductive capping layer over all of the copper layer, with none of the capping layer over any of the dielectric structures.

19. The integrated circuit of claim 18, wherein the capping layer is at least partially above the upper level of the dielectric structures.

20. The integrated circuit of claim 18, wherein the electrically conductive capping layer comprises an alloy of at least one of cobalt and nickel.